

Amendments to the Drawings:

The attached replacement sheets of drawings includes changes to Figs. 1, 3 and 4 and replaces the original sheets including Fig. 1, 3 and 4.

Figure 1 has been amended to correct the label PB7 to read PB8. Figures 1, 3 and 4 have also been amended to include the missing labels PB6, PB7, PB10, PB11 and PB12. Figures 3 and 4 have been amended to include the missing labels PB8, PB14, PB15 and PB16.

Attachments following last page of this Amendment:

Replacement Sheets (2 pages)

REMARKS

Status of the Application

Claims 1-6 are pending in this application. Claim 1 is the sole independent claim.

The office action:

- i. objected to drawings 1-4 because the drawings were allegedly not provided with descriptive text labels,
- ii. rejected Claims 1-3, 5 and 6 under 35 USC 103 as allegedly being unpatentable over US 5,289,470 to Chang et al (Chang) in view of US 6,032,190 to Bremer et al (Bremer), and
- iii. objected to Claim 4 as being dependent on a rejected claim, but noted its allowability if rewritten in independent form (which indication is appreciatively noted).

In this response, the applicant has corrected the drawings to provide descriptive text labels, and has provided remarks to traverse the rejection. Reconsideration and allowance of the present application are respectfully requested.

Background

The present application relates to a data switch that includes memory, which is divided into packet buffers, and a plurality of registers. The data switch also includes a control unit that checks if a received data packet meets a criterion for efficient storage in the packet buffers. If the packet cannot be efficiently stored, the control unit divides the packet into a first portion that is stored in the packet buffers and a second portion that is stored in the registers.

Objection to Drawings

The rejection found the drawings to lack descriptive labels. The applicant understands that the objection relates to the lack of labels for some of the boxes illustrated in the drawings. The applicant has now provided the appropriate labels for the boxes. Support for the labels can be found, for example, in page 1 lines 27-28.

Rejection of Claims: 35 USC 103

The rejection found Chang to disclose all of the features of independent Claim 1, except the feature of storing a second portion of a data packet into a plurality of registers. The examiner found this feature in Bremer, and concluded that it would have been obvious to one of ordinary skill in the art to

modify Chang to implement the feature from Bremer. The applicant respectfully traverses this rejection.

The applicant submits that the combination of Chang and Bremer is based on impermissible hindsight (i.e. based on knowledge gleaned from the present application). There is no teaching, suggestion or motivation in the two documents that would point one of ordinary skill in the art to bring them together. Furthermore, there would have been no reason for one of ordinary skill in the art to combine the two documents. The reasoning for combining the two documents appears to be that a skilled person considering Chang and Bremer would have noted Bremer's registers that provide 'quicker access', and this would have prompted the skilled person to modify Chang to include Bremer's registers 'for the benefit of improving buffer memory utilization'. The applicant respectfully disagrees. A person skilled in the art, starting from Chang and looking to improve buffer memory utilization, would not find Bremer helpful since Bremer is directed at removing the header portion of a data packet and appropriately processing the header portion to 'significantly reduce the time required to process and route a data packet' (see Bremer column 4 lines 30-33). Bremer's use of registers for 'quicker access' is unrelated to Chang's goal of flexible 'buffer memory utilization'.

Even if, assuming for argument's sake, Chang and Bremer can be properly combined, the combination does not disclose each and every element of independent Claim 1 of the present application. For example, Claim 1 requires 'a control unit for determining whether a data packet ... meets a criterion for efficient storage in the packet buffers and otherwise dividing the data packet...'. Neither Chang nor Bremer suggest such a control unit. The rejection states that Chang discloses the comparison of a packet with a buffer size, and concluded that this was equivalent to the control unit of Claim 1. The applicant disagrees. Chang does not disclose any comparison of the packet size with the buffer size. In fact, Chang does not mention the term 'compare' or any of its derivatives. Chang simply directs all portions of a data packet into an allocated buffer. If the allocated buffer is found to be full, Chang directs the remaining portions of the packet to another buffer. No comparison of the packet size and buffer size is carried out as suggested by the examiner. It follows that Chang does not disclose determining whether a data packet meets a criterion for efficient storage in the packet buffers.

Furthermore, if Chang and Bremer can be properly combined as above, the combination would effectively teach away from the invention claimed in Claim 1. For instance, Chang teaches only the use of packet buffers to store data packets. If a data

packet is too big to be stored in one packet buffer, another (possibly different-sized) *packet buffer* is allocated. This is contrary to the requirement of claim 1 of storing a second portion of the data packet in registers. As for Bremer, it teaches separating a packet's header portion and data portion, where the header portion is stored in registers, and the data portion is stored in a buffer. This is done regardless of the size of the data packet. So if the data packet has a large data portion, it is still stored in the buffer, *regardless of whether the storage is an efficient storage in the buffer*. Bremer's teaching is therefore contrary to the feature of claim 1, where a control unit divides a data packet *on the basis of whether or not it meets a criterion for efficient storage in the packet buffers*. If the teachings of Chang and Bremer are combined, one of ordinary skill in the art is likely to arrive at a solution where the header portion of a data packet is always stored in a register (following Bremer's teaching for fast access) and the data portion of the packet is always stored in the buffer, where different-sized buffers are used to optimize buffer use (following Chang's teaching of buffer use). Such a solution is, however, contrary to what is recited in claim 1.

Allowable Subject Matter

The applicant acknowledges with appreciation the indication that claim 4 recites patentable subject matter and would be allowable if rewritten in independent form to include all of the features of its base claim. The applicant has maintained claim 4 in dependent form because it is believed that its base claim (i.e. claim 1) is patentably distinguished over the cited art, for at least the reasons discussed in this paper.

Applicant asks that all claims be allowed. No fee is believed to be due, however please apply any credits or additional charges to deposit account 06-1050.

Respectfully submitted,

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